Implementation of an Experimental 384 kb/s Radio Link for High-Speed Internet Access
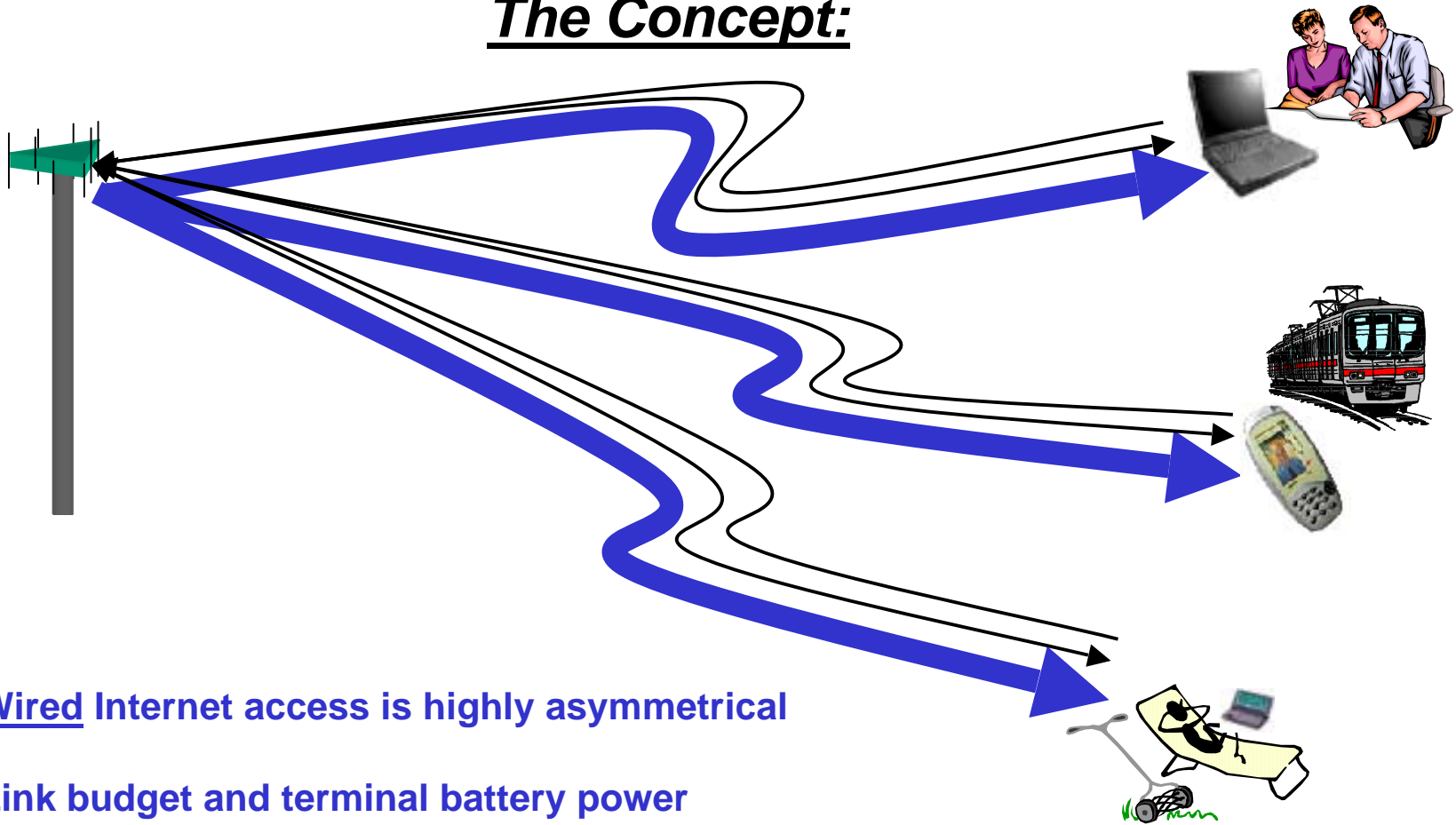
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**AT&T Labs - Research
Wireless Systems Research
Red Bank, NJ**

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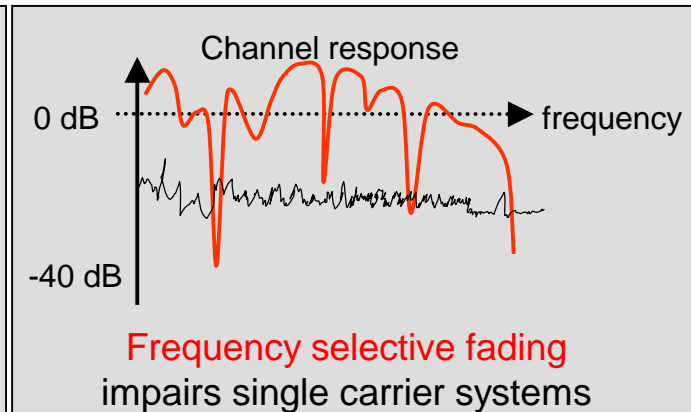**Wireless Systems Research**

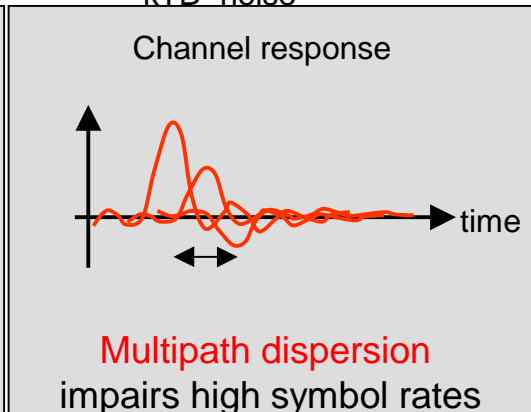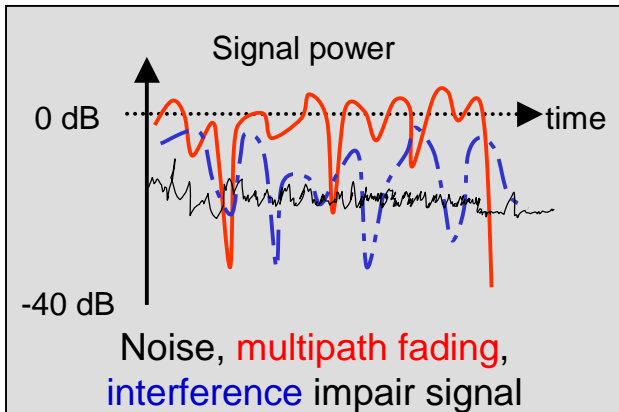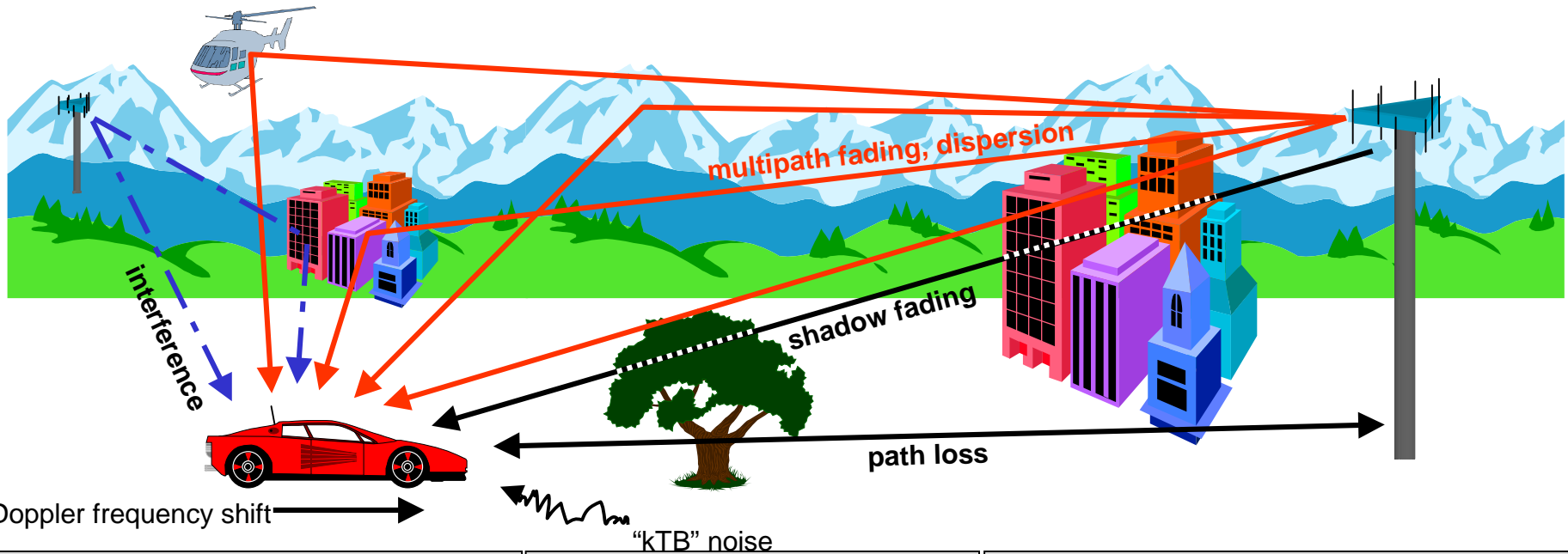# 4G Wireless
The Concept:

- **Wired Internet access is highly asymmetrical**

- **Link budget and terminal battery power constrain uplink speed**
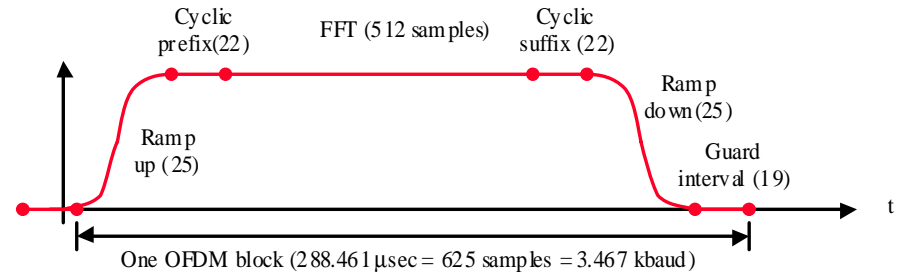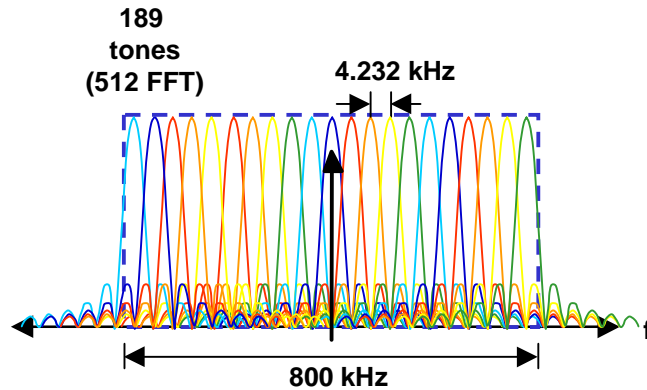
Overlay a high speed downlink on "existing" two-way systems

High Speed Data Networking in a
High Mobility, Wide Area, Cellular-like Environment
The Challenge:

multipath fading, dispersion

interference

shadow fading

path loss

Doppler frequency shift

"kTB" noise

Signal power	Channel response	Channel response
0 dB → time	→ time	0 dB → frequency
-40 dB		-40 dB
Noise, multipath fading, interference impair signal	Multipath dispersion impairs high symbol rates	Frequency selective fading impairs single carrier systems

OFDM for High Speed Wireless Data Networking

OFDM Transmitter
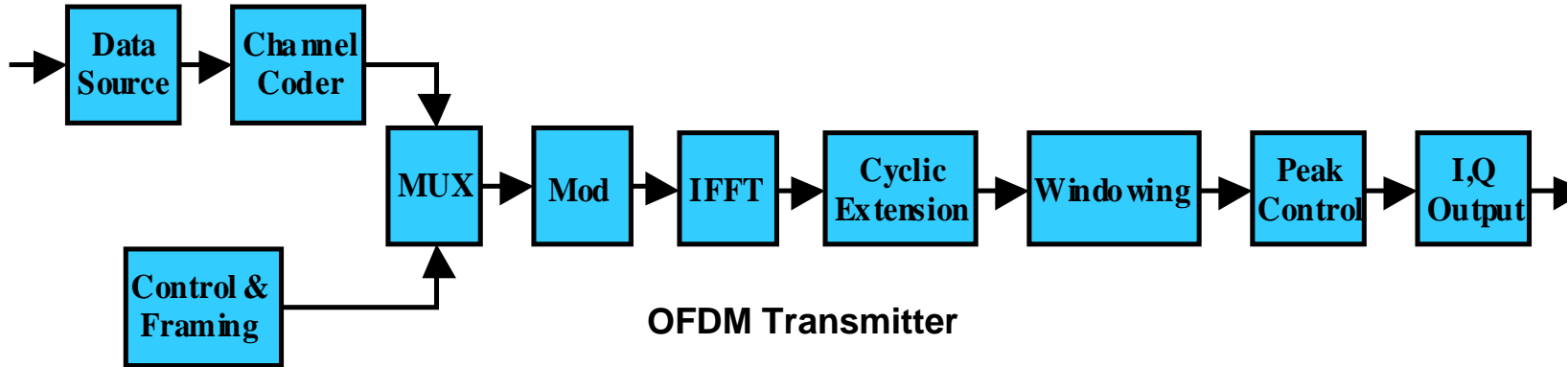
- **Low symbol rate (~3.5 kbaud) protects against changing mobile channel**
- **Sparse constellation on each carrier (QPSK) provides resistance against noise**
- **Coding across tones provides frequency diversity**
- **Large number of carriers provides high capacity (189 user bits/288 μsec ~544 kb/s)**

OFDM Experimental Hardware
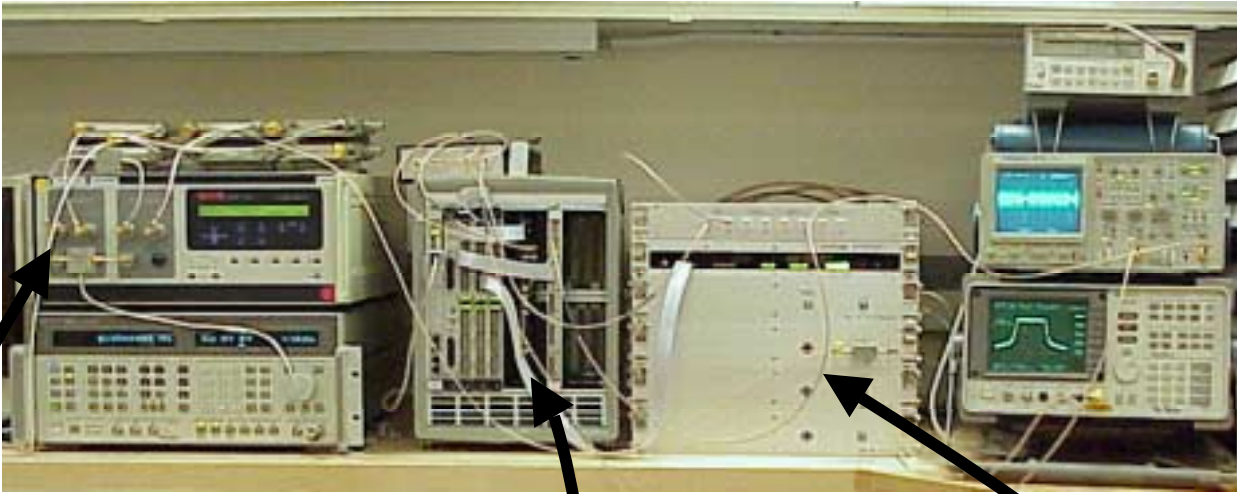
- Baseband signal processing based on commercial off-the-shelf DSP hardware with some custom designed components
- 1900 MHz transceiver
- Real-time performance measured through RF fading simulator
- System parameters:
    - >384 kb/s end user data rate
    - 800 kHz downlink bandwidth
    - GSM-derived clock rates
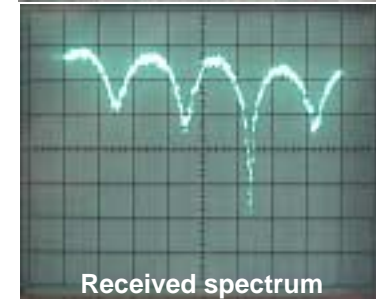
Received spectrum

Demod constellations

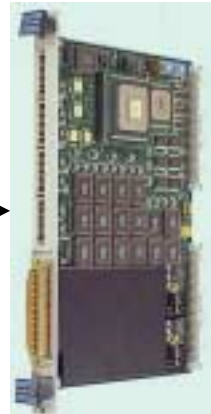AT&T
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OFDM Prototype

RF

RF interface

Pentek A/D

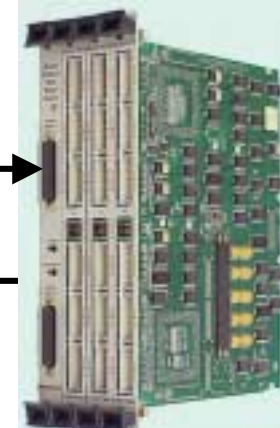**Pentek 'C40 DSPs**
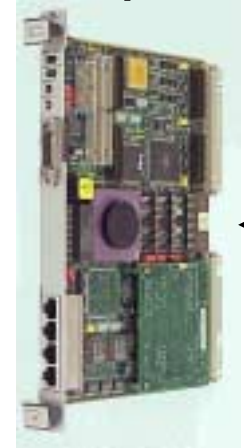
Pentek Node Controller

- **PCS band operation**
- **384 kb/s end user capacity in 800 kHz**
- **with OFDM**
- **DSPs programmed (mostly) in C**
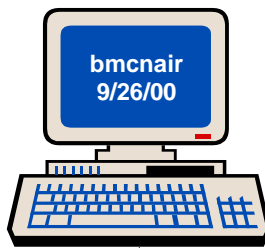- **Experiment with 2-way diversity, synchronization**

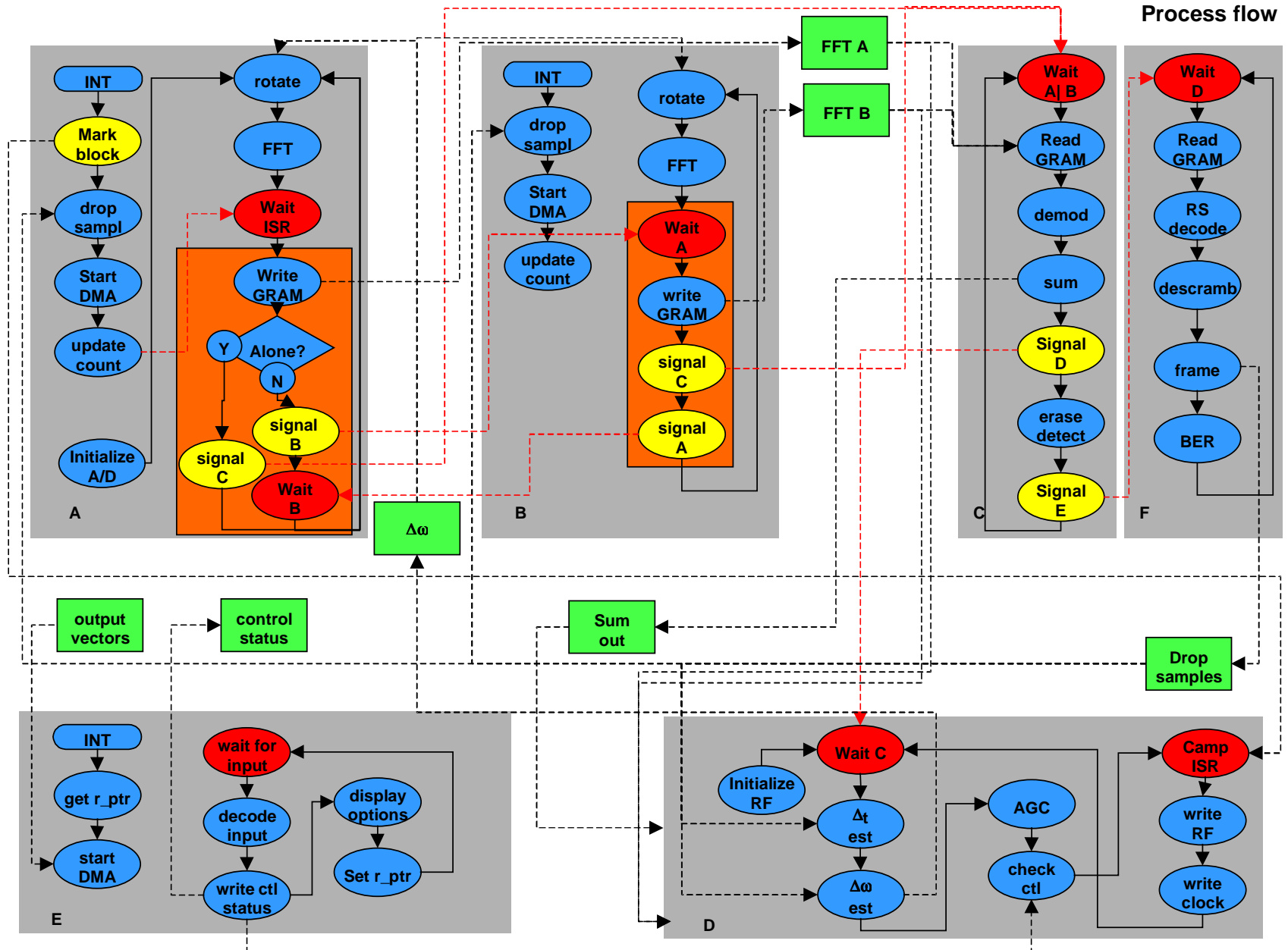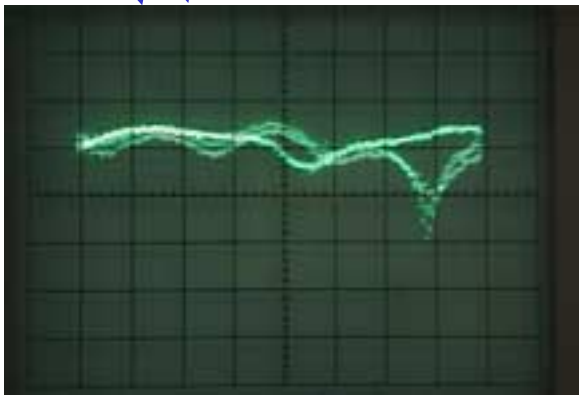**Custom D/A**

Custom Clock Board

bmcnair
9/26/00

Sun development platform

OFDM Receiver - DSP Hardware Architecture
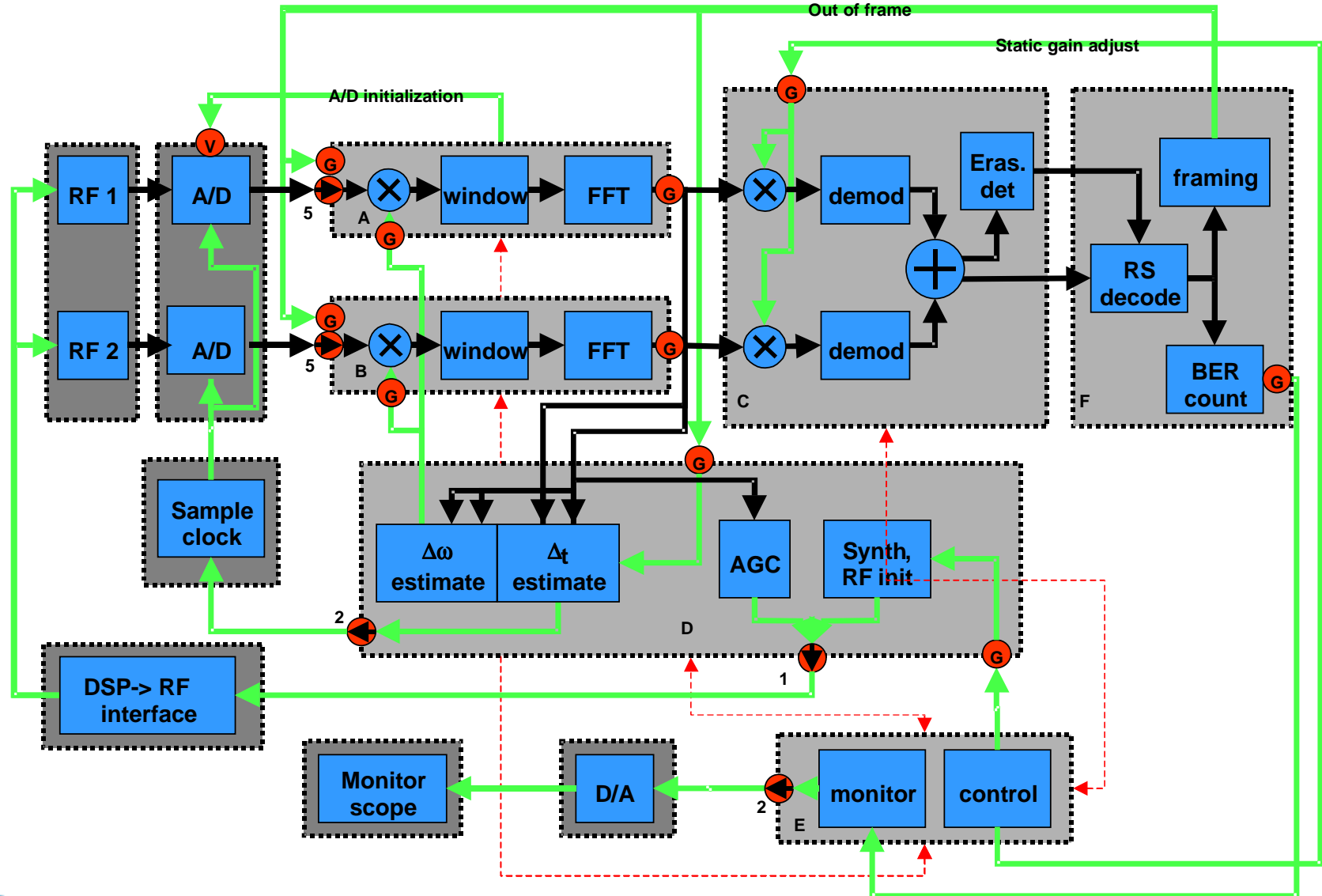
OFDM Receiver - DSP Software Architecture

Process flow

A

- INT
- Mark block
- drop sampl
- Start DMA
- update count
- Initialize A/D
- rotate
- FFT
- Wait ISR
- Write GRAM
- Alone? — Y / N
- signal B
- signal C
- Wait B

B

- INT
- drop sampl
- Start DMA
- update count
- rotate
- FFT
- Wait A
- write GRAM
- signal C
- signal A

FFT A

FFT B

Δω

C

- Wait A| B
- Read GRAM
- demod
- sum
- Signal D
- erase detect
- Signal E

F

- Wait D
- Read GRAM
- RS decode
- descramb
- frame
- BER

output vectors

control status

Sum out

Drop samples

E

- INT
- get r_ptr
- start DMA
- wait for input
- decode input
- write ctl status
- display options
- Set r_ptr

D

- Wait C
- Initialize RF
- Δt est
- Δω est
- AGC
- check ctl
- Camp ISR
- write RF
- write clock

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Real-time displays from
"Typical Urban" channe

1 Hz fading for illustrationl

800 kHz

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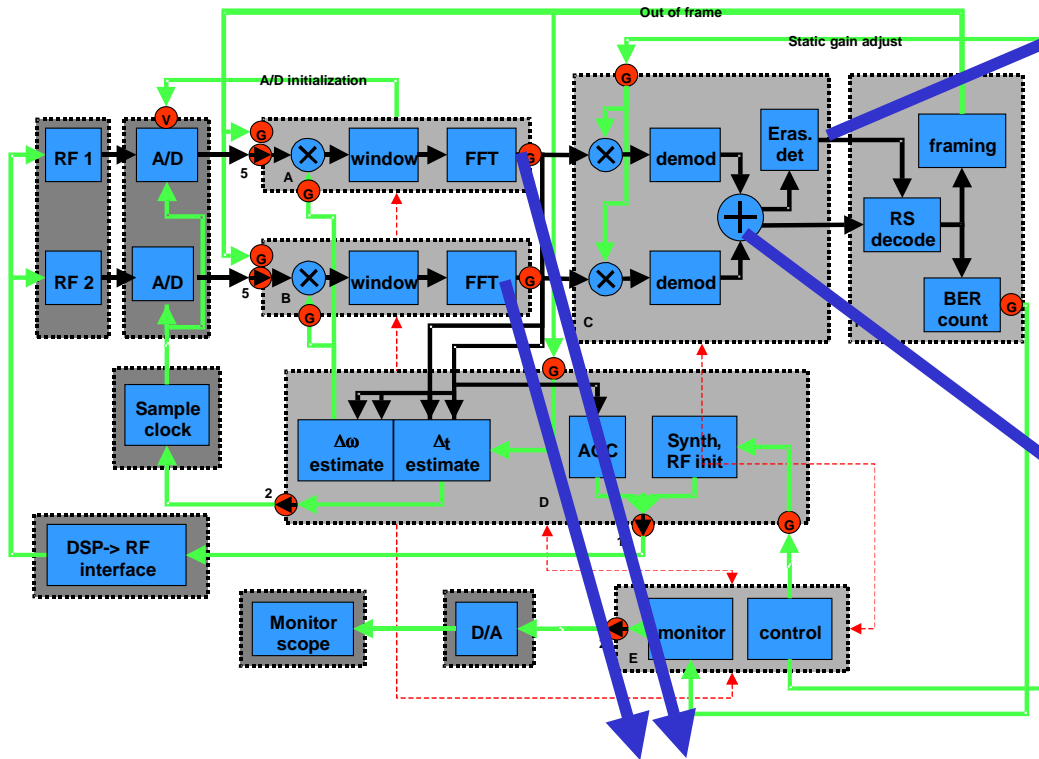
Simulated vs. Measured Results

Legend:
- measured: 2rx, 200Hz, 20usec
- measured: 2rx, 200Hz, 5usec
- measured: 2rx, 40Hz, 20usec
- measured: 2rx, 40Hz, 5usec
- simulation: 2rx 200Hz 20usec
- simulation: 2rx 200Hz 5usec
- simulation: 2rx 40Hz 20usec
- simulation: 2rx 40Hz 5usec

FER vs. SNR (dB)

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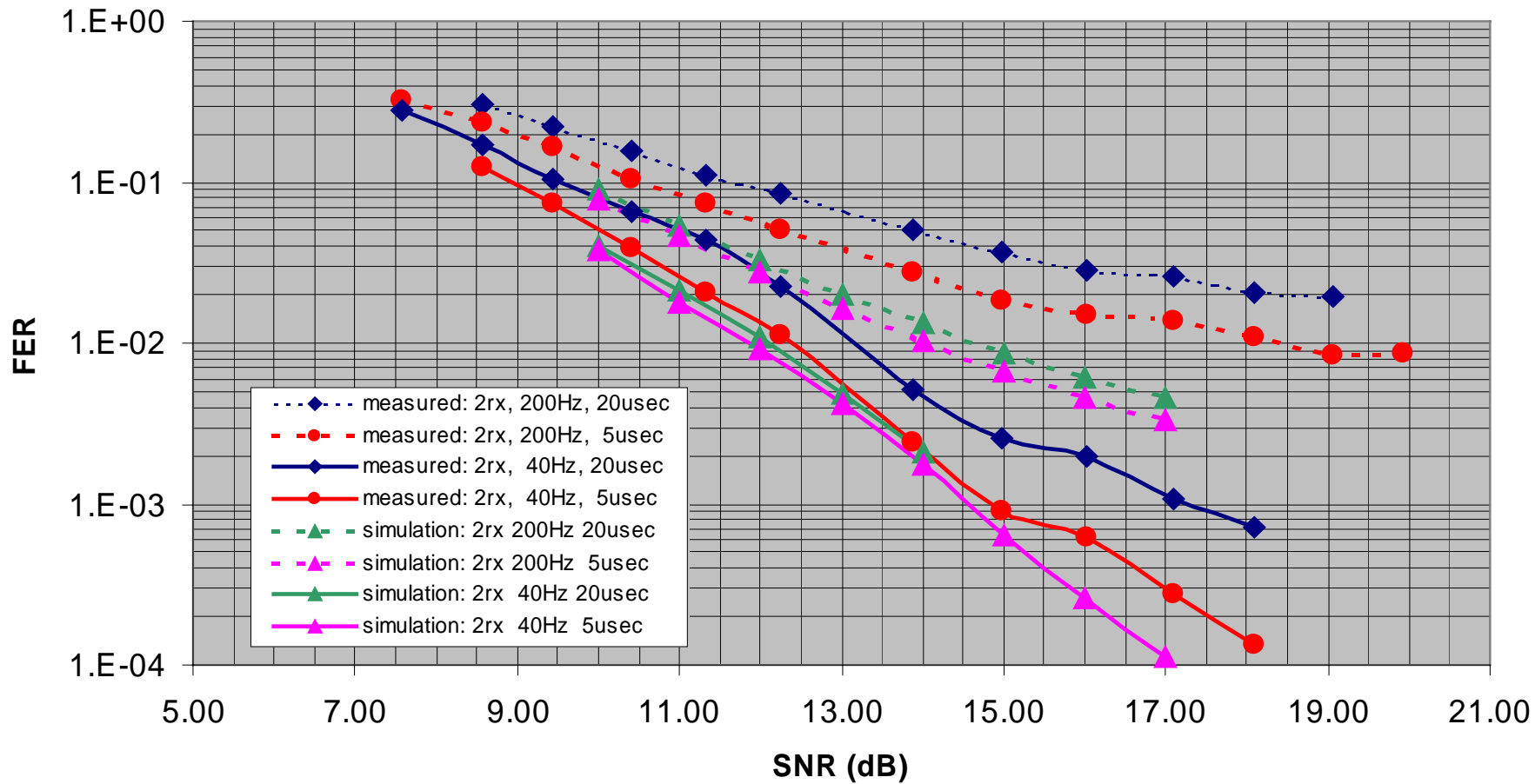
Conclusions

- A real-time prototype of a 384 kb/s OFDM system for operation at PCS frequencies has been completed and tested in high-mobility settings

- Real-time DSP prototype demonstrated:
    - close agreement between theory/simulation and implementation
    - robustness of OFDM against delay spread
    - robustness of differential-in-frequency timing estimation

- OFDM can offer good performance with straightforward receiver (e.g., simple combining, differential detection, (63,31) RS coder)

- Two-branch receiver diversity offers significant performance gain for variety of channel conditions, especially paired with coding across frequency

- Continuing work is focused on 5-10 Mb/s with similar mobility

- Come to tomorrow afternoon's talk to hear more about performance of the 384 kb/s system